

# Sungyu Jeong

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## EDUCATION

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- M.S.-Ph.D. Combined** Pohang University of Science and Technology (POSTECH), Korea Feb. 2018–Feb. 2026  
Electrical Engineering, Advisor: Prof. Byungsub Kim (Expected)  
Dissertation: "Methodologies for Analog Layout Design Automation"
- B.S.** Pohang University of Science and Technology (POSTECH), Korea Mar. 2014–Feb. 2018  
Electrical Engineering

## RESEARCH INTERESTS

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Analog and mixed-signal circuit design automation with focus on:

- Foundation models and self-supervised learning for analog circuit design.
- Layout-native data representation for efficient deep learning on physical layouts.
- Multi-modal pre-training integrating schematic and layout modalities.
- Procedural layout generation and layout-to-generator conversion frameworks.
- GUI-based EDA tools bridging manual design expertise and automation.

## PUBLICATIONS AND PATENTS

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*J=Journal, C=Conference, P=Patent*

- [J1] S. Jeong, W. J. Choi, J. Choi, A. Biswas, and B. Kim, "A Self-Supervised Learning of a Foundation Model for Analog Layout Design Automation," *IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)*, pp. 1–11, 2025.
- [J2] S. Jeong et al., "A Layout-to-Generator Conversion Framework With Graphical User Interface for Visual Programming of Analog Layout Generators," *IEEE Access*, vol. 12, pp. 125942–125954, 2024.
- [C1] S. Han, S. Jeong, C. Kim, H.-J. Park, and B. Kim, "GUI-Enhanced Layout Generation of FFE SST TXs for Fast High-Speed Serial Link Design," in *2020 57th ACM/IEEE Design Automation Conference (DAC)*, July 2020.
- [P1] B. Kim and S. Jeong (2024). COMPUTING DEVICE AND METHOD FOR ASSIGNING GENERATOR TO SEMICONDUCTOR LAYOUT AND METHOD OF TRAINING NEURAL NETWORK. U.S. Patent Application, Application No. US18/652,685. Filing Date: 2024-05-01, Publication No. US20240370620A1, Publication Date: 2024-11-07.
- [P2] B. Kim and S. Jeong (2024). USER INTERFACE METHOD OF SEMICONDUCTOR DESIGN PROGRAM AND OPERATION DEVICE THEREFOR. U.S. Patent Application, Application No. US18/651,601. Filing Date: 2024-04-30, Publication No. US20240370614A1, Publication Date: 2024-11-07.

## RESEARCH EXPERIENCE

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- 1. Machine Learning-Based Design Automation/Optimization Software Development** 2024–2025  
**& AI-Driven Analog Circuit Design and Layout Efficiency/Automation** 2025–Present  
**Strategic Industry-Academia Collaboration Project Funded by Samsung Electronics Company Ltd.**

*Project: Foundation Model for Analog Layout Design Automation*

- Proposed foundation model for analog layout design automation.
- Designed self-supervised learning methodology for analog layout data.
- Developed generative model for layout element generation, including analog cell metal routing, N-well and dummy finger generation, and via/contact insertion.
- Developed CNN-based classifier for automatic sub-cell layout identification.

**2. Analog IP Translational Research Lab Utilizing Layout Automation Software  
Funded by the Ministry of Science and ICT (MSIT) of Korea**

2021–2023

*Project: GUI-Based Layout-to-Generator Conversion Framework Development*

- Developed GUI-based framework for converting existing layouts into procedural layout generators.
- Developed layout generators of high-speed wireline receiver, DCDL, and DCC circuits.
- Reduced procedural layout development time by 55% (from 44.5 hours to 20 hours).
- Achieved RX layout instance generation time of less than 0.3 seconds, achieving 20 Gbps error-free data reception on post-layout simulation.
- Filed international patents (KR, US, EU, CN) for user interface method of semiconductor design program [P2].

**3. Automatic Design Generation of Ultra High-Speed I/O Circuit to Support Intelligent Semiconductor Devices  
Funded by the National Research Foundation of Korea**

2019–2021

*Project: Designing High-Speed Wireline Transmitter Using Layout Generator*

- Developed procedural layout generation engine for analog layout design automation.
- Codified procedural layout generator with silicon-proven result on 65 nm, and post-layout simulation verification 40 nm, and 90 nm process nodes.
- Achieved core generation time of less than 30 minutes with automated layout flow.
- Demonstrated 8 Gbps operation under 20 dB channel loss condition.
- Published in ACM/IEEE Design Automation Conference (DAC) 2020 [C1].

**HONORS AND AWARDS**

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- [A1] Grand Prize (Minister's Award), 12th G-Star University Startup Competition, Ministry of SMEs and Startups 2023  
[A2] Excellence Prize (POSTECH Holdings CEO Award) & Popularity Prize, POSTECH Startup Competition 2023  
[A3] POSTECH Alchemist Fellowship, Pohang University of Science and Technology 2023  
[A4] President's Prize (ETRI), Korea Semiconductor Design Competition 2020  
[A5] National Science and Engineering Undergraduate Scholarship, Ministry of Science and ICT 2016, 2017

**EXPERIENCES**

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<b>Poster Presenter</b>	<b>Design Automation Conference (DAC), Work-in-Progress (WIP)</b> “A CNN-Based Code Assistance for Layout-to-Generator Conversion of Analog Circuits”	2023
<b>Young Professional</b>	<b>Design Automation Conference (DAC)</b> Participated in DAC Young Professional program	2020, 2023
<b>Startup Program</b>	<b>Pohang Innopolis Campus, POSTECH &amp; Ministry of Science and ICT</b> Participated in entrepreneurship education and startup capability training	2023–2024
<b>Military Service</b>	<b>Technical Research Personnel,</b> Republic of Korea Army	2021–2024
<b>Teaching Assistant</b>	<b>Pohang University of Science and Technology (POSTECH), Korea</b> Basic Circuit Experiments (EECE 281)	2018

**SKILLS**

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<b>Technical Skill</b>	Programming Languages: Python, C / C++, SKILL, Qt (PyQt, PySide) Data Science & Machine Learning: PyTorch, TensorFlow, Keras, MATLAB, R Circuit Design & EDA Tools: Spectre, Virtuoso, Calibre, HSPICE
<b>Languages</b>	Korean, English

**REFERENCES**

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**Prof. Byungsub Kim** Professor in Department of Electrical Engineering  
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